Proceedings of 8th Thin Film Materials & Devices Meeting
November 4-5, 2011, Kyoto, Japan
http://www.tfmd.jp/

Improvement in Electrical Characteristics of Microcrystalline Silicon Thin Film Transistors by High-pressure H_2O vapor Heat Treatment

A. Shuku[1], E. Takahashi[1], Y. Andoh[1], Y. Nagatomi[2], and T.Sameshima[2]

[1] NISSIN Electric Co., Ltd, 47, Umezu-Takase-cho, Ukyo-ku, Kyoto, 615-8686, Japan
[2] Tokyo University of Agriculture and Technology, 2-24-16, Naka-cho, Koganei, Tokyo, 184-8588

Keywords: uc-Si, ICP, PECVD, TFT

Abstract. Thin film transistors (TFTs) with no doped source and drain regions were fabricated in microcrystalline silicon (μc-Si) films formed at 125, 150, and 200 °C using inductively coupled plasma chemical vapor deposition (ICP-CVD). Transfer characteristics for as fabricated TFTs with μc-Si in every deposition condition showed typically n-type and depletion type behavior. $1x10^6$ Pa H_2O vapor heat treatment at 260 °C for 3 h changed transfer characteristics to enhancement type ones for TFTs fabricated in μc-Si films formed at 150 and 200 °C, respectively. The threshold voltages for TFT with μc-Si formed at 125, 150, and 200 °C were -6 ,0.5 and -0.5 V, respectively. Furthermore, the high-pressure H_2O vapor heat treatment markedly decreased the hysteresis voltage width in transfer characteristics into 0.5, 1.0 and 0.5 V for μc-Si formed at 125, 150, and 200 °C, respectively.

Introduction

Microcrystalline silicon (μc-Si) films have high field effect mobility compared with amorphous silicon (a-Si) films. They can be formed at a low temperature by using plasma enhancement chemical vapor deposition (PECVD). μc-Si films have been therefore researched and developed for a long time for application of them to fabrication of thin film transistors (TFTs) at low temperatures [1, 2]. The excimer laser annealing (ELA) method has been standardized for forming polycrystalline silicon films. It has been applied to production of poly-Si TFT electronic circuits for liquid crystal display (LCD) and organic electroluminescence (EL) display devices [3]. We believe that μc-Si still is a promising material because of advantage of the simply direct deposition for fabricating TFTs with rather high field effect mobility for large-size-display-device production.

We have developed inductively coupled plasma (ICP) CVD equipment which has the potential to synthesize good quality μc-Si film thanks to low plasma damage resulting from a high plasma density ($1x10^{12}$ cm^{-3}) and a low plasma potential (<40 V).

Moreover, we have also developed high-pressure H_2O vapor heat treatment to improve TFT characteristics. High-pressure H_2O vapor heat treatment has improved laser-crystallized TFT characteristics at low temperatures below 300 °C [4, 5, 6]. The defect reduction of the μc-Si films has been achieved via a hydrothermal synthesis reaction under high pressure and high temperature.

In this paper, we report on μc-Si TFT fabrication at low temperatures of 125, 150 and 200 °C as temperatures of μc-Si formation. We also report improvement in TFT characteristics using high-pressure H_2O vapor heat treatment at 260 °C. In particular, we concentrate changes in the threshold voltage and the hysteresis behaviors in transfer characteristics.

Experimental procedure

Undoped 50-nm-thick μc-Si films were synthesized by the ICP-CVD method on 0.02 Ωcm n

type crystalline silicon substrates with both surfaces coated with 100-nm-thick thermally grown silicon dioxide (SiO_2) layers. The substrate temperature was set at 125, 150 and 200 ^oC. A 13.56-MHz radio-frequency (RF) power was applied at 7.5 kW. A mixed gas of SiH_4 at 100 sccm and H_2 at 150 sccm was flowed with a pressure of 0.67 Pa. Contact holes were subsequently opened in the μc-Si and SiO_2 layers by reactive-ion etching (RIE) to use crystalline silicon substrate as the gate electrode, as shown in Fig. 1(a). The 300-nm-thick Al metal films were then deposited and defined as source, drain, and gate electrodes using the liftoff method. μc-Si islands were finally defined as channel areas by RIE, as shown in Fig. 1. As shown in a plane and top view of our μc-Si TFT in Fig. 2 all of Al electrodes were formed on the top surface because of experimental measurement matter of TFT characteristics.

μc-Si TFTs were then annealed by $1x10^6$ Pa H_2O vapor heat treatment at 260 ^oC for 3 h with equipment shown in Fig. 3. The pressure was determined from a process temperature, a chamber volume and a water volume.

TFT characteristics were measured in the dark field at a step time of 0.2 s and a drain voltage of 0.1 V.

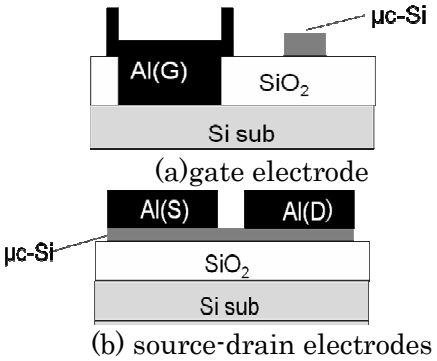

Fig.1 Schematic cross section of bottom gate μc-Si TFT

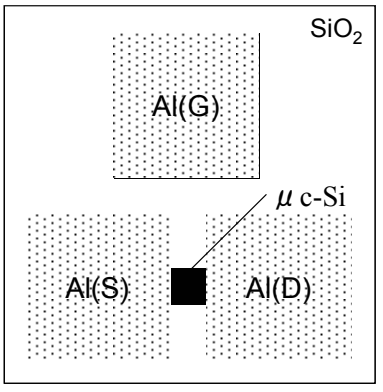

Fig.2 Plane view of bottom gate μc-Si TFT

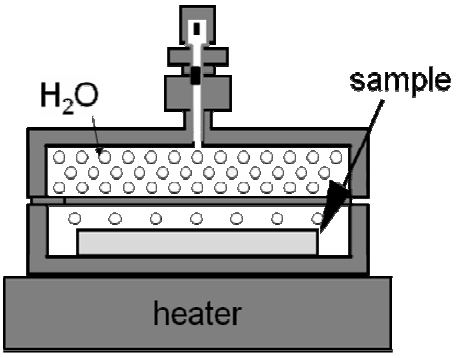

Fig.3 High-pressure H_2O vapor heat treatment

Results and Discussion

TFTs with μc-Si films formed at 125, 150 and 200 ^oC showed typical n-type transfer characteristics, as shown in Fig. 3(a), (b), and (c), respectively, while TFTs had no doped source and drain regions, as shown in Fig. 1. Hole current did not appear in negative gate voltage regions. Those characteristics shown in Fig. 3 suggest that the effective hole mobility might be extremely low if hole carriers were accumulated via change in the band potential of the μc-Si

caused by the negative gate voltage according to simple MOSFET theory [7].

Substantial drain current flowed by applying the gate voltage above -10V. The negative fixed charges probably existed at SiO_2/Si interfaces or μc-Si layers. Furthermore, the drain currents in the case of gate voltage application from negative to positive (forward direction) were lower than that in the case of gate voltage application from positive to negative (reverse direction). Those hysteresis phenomena indicate transient negative charge accumulation in μc-Si layer caused by applying the gate voltage [8].

On the other hand, $1x10^6$-Pa-H_2O-vapor heat treatment at 260 ^oC for 3 h markedly changed transfer characteristics. The drain current curves shifted to the positive voltage direction, as shown in Fig. 3 (b) and (c). The shift of transfer characteristics was evaluated as the change in the threshold voltage V_t, in the case of forward gate voltage application. The initial V_t for TFTs with μc-Si films formed at 125, 150 and 200 ^oC were -3, -2, and -2 V, respectively. The high-pressure H_2O vapor heat treatment changed V_t to -6, 0.5, and -0.5 V, respectively. The changes in V_t were therefore -3, 2.5 and 1.5 V, respectively, as shown in Table I. It is interesting that $1x10^6$-Pa-H_2O-vapor heat treatment at 260 ^oC for 3 h was effective in changing transfer characteristics to enhancement type ones only for μc-Si deposition temperatures of 150 and 200 ^oC.

Moreover, $1x10^6$-Pa-H_2O vapor heat treatment increased the drain current in the high negative gate bias region for every TFT, as shown in Fig. 3. We interpret that high-pressure H_2O vapor heat treatment increased the effective hole mobility.

Furthermore, $1x10^6$-Pa-H_2O-vapor heat treatment at 260 ^oC for 3 h reduced hysteresis characteristics in transfer characteristics for every TFT, as shown in Fig. 3. The transfer characteristics in forward and reverse directions became almost the same. We evaluated hysteresis voltage width (ΔV) as the voltage difference between V_t (forward voltage application case) and V_r, which was a voltage giving the same drain current for reverse voltage application as that at V_t ($\Delta V=V_t-V_r$). ΔV of initial TFTs with μc-Si films formed at 125, 150 and 200 ^oC was 2.0 V. $1x10^6$-Pa-H_2O-vapor heat treatment at 260 ^oC for 3 h decreased ΔV to 0.5, 1.0, and 0.5 V, respectively, as shown in Table I. Those results indicate that $1x10^6$-Pa-H_2O-vapor heat treatment at 260 ^oC for 3 h reduced the transient charge accumulation in μc-Si films.

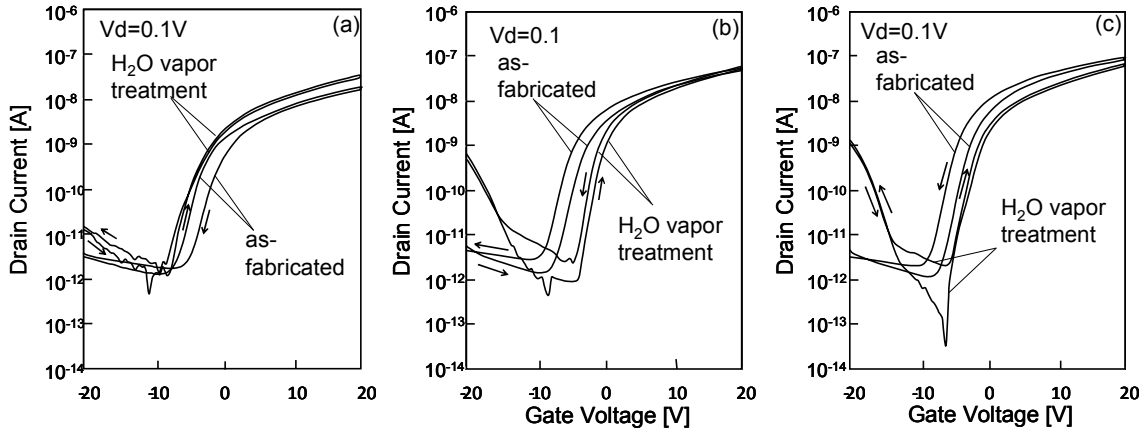

Fig.3 Transfer characteristics of as-fabricated and $1x10^6$ Pa H_2O vapor heat treatment at 260 ^oC for 3 hours for TFTs with μc-Si films formed (a) at 125 ^oC, (b) at 150 ^oC, and (c) at 200 ^oC.

Table I. Vt and Δ V in transfer characteristics at 125, 150, 200 °C.

	Substrate temperature[℃]	As-fabricated	H_2O vapor heat treatment
Threshold voltage[V]	125	-3.0	-6.0
	150	-2.0	0.5
	200	-2.0	-0.5
Hysteresis voltage width[V]	125	2.0	0.5
	150	2.0	1.0
	200	2.0	0.5

Figures 4, 5, and 6 show output characteristics of as-fabricated TFTs for μc-Si formed at 125, 150 and 200 °C, respectively. (a) and treated with $1x10^6$-Pa-H_2O-vapor heating at 260 °C for 3h (b). Output characteristics showed n-type ones with good ohmic behaviors for every TFT. The drain current was highest in the case of μc-Si formation at 200 °C. The $1x10^6$-Pa-H_2O-vapor heat treatment at 260 °C for 3 h increased the drain current at 125 and 150 °C by 278 and 130 %

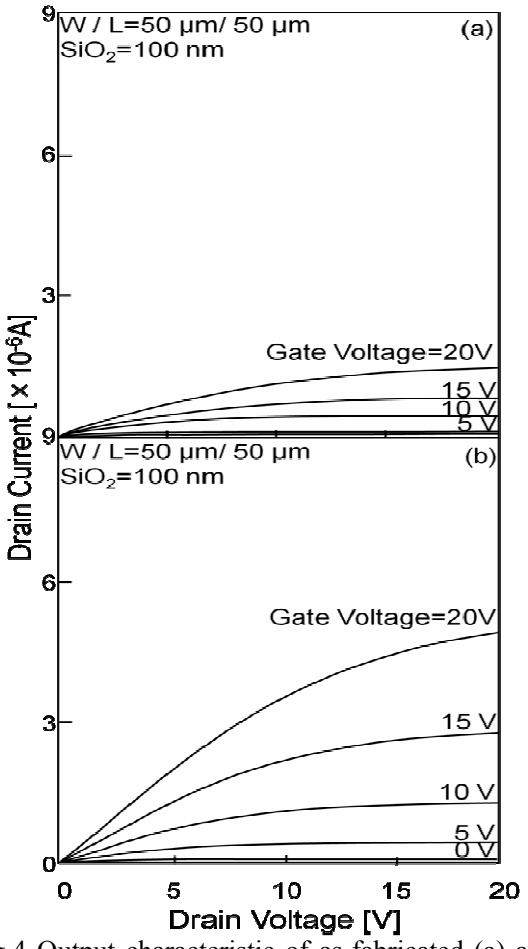

Fig.4 Output characteristic of as-fabricated (a) and $1x10^6$ Pa H_2O vapor heat treatment at 260 °C for 3 hours (b) for TFTs with μc-Si films formed at 125 °C

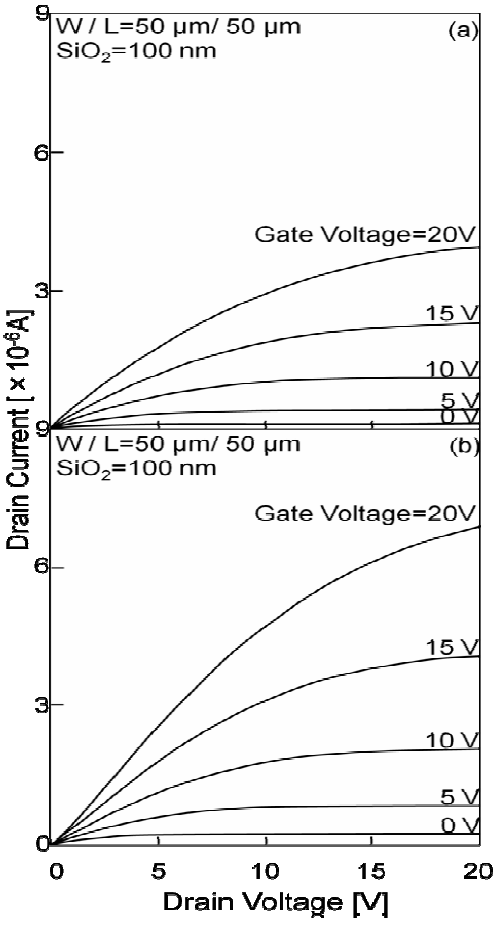

Fig.5 Output characteristic of as-fabricated (a) and $1x10^6$ Pa H_2O vapor heat treatment at 260 °C for 3 hours (b) for TFTs with μc-Si films formed at 150 °C

at gate and drain voltages of 20 V. The highest drain current shows that high electrical conductance was achieved for high temperature deposition. We believe that high deposition temperature resulted in a low density of crystalline defects associated with a low potential barrier height.

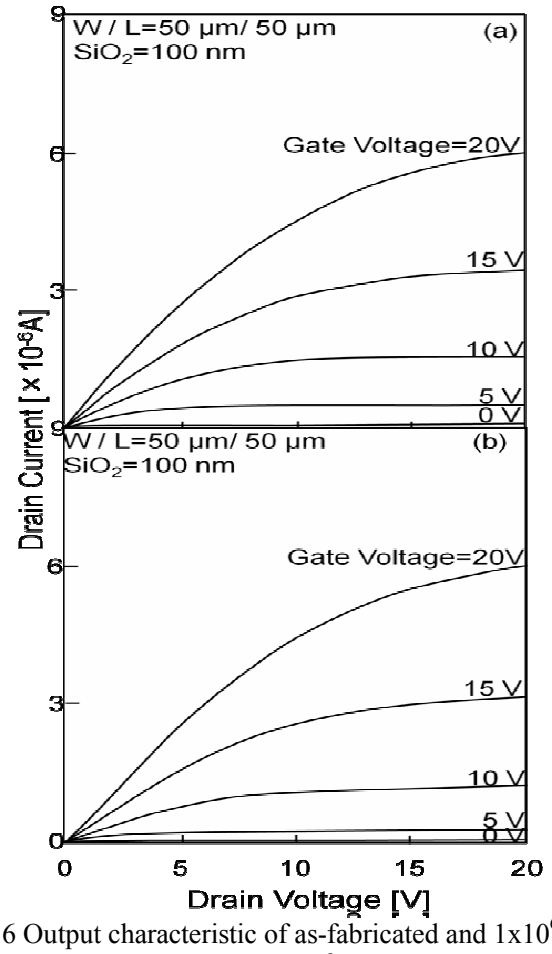

Fig.6 Output characteristic of as-fabricated and $1x10^6$ Pa H_2O vapor heat treatment at 260 °C for 3 hours (b) for TFTs with μc-Si films formed at 200 °C

Summary

Bottom-gate type TFTs were fabricated in μc-Si films formed at 125, 150, and 200 °C using ICP-CVD. V_t at a drain voltage of 0.1 V for TFTs with μc-Si formed at 125, 150 and 200°C were -3, -2 and -2 V, respectively. $1x10^6$-Pa-H_2O-vapor heat treatment at 260°C for 3 h changed V_t to -6, 0.5, and -0.5 V, respectively. Furthermore, the treatment markedly decreased hysteresis voltage width in transfer characteristics from 2.0 V (initial) to 0.5, 1.0 and 0.5 V for μc-Si formed at 125, 150 and 200 °C, respectively. The high-pressure H_2O vapor heat treatment was effective for reducing hysteresis characteristics.

References

[1] M. Kondo , M. Fukawa, L. Guo, A. Matsuda: J. Non-Crystal. Sol.266-269 (2000) 84.
[2] A. Matsuda: J. Non-Crystal. Sol 338–340 (2004) 1.
[3] J. Jang: Proc. in Workshop on Active Matrix Liquid Crystal Displays, (Tokyo Japan, 2002) 5
[4] T.Shimoda: Proc. In Workshop on Active Matrix Liquid Crystal Displays, (Tokyo Japan, 2002) 5
[5] H. Watakabe and T. Sameshima: Jpn. J. Appl. Phys. 41(2002) L974.
[6] Katsumi ASADA, Keiji SAKAMOTO, Tadashi WATANABE, Toshiyuki SAMESHIMA and Seiichiro HIGASHI: Jpn. J. Appl. Phys. 39(2000) pp. 3883-3887.
[7] A. S. Grove: Physics and Technology of Semiconductor Devices (Wiley, New York, 1967) Chap. 9.
[8] Y.Urabe, T. Sameshima, K. Motai and K. Ichimura: Jpn. J.Appl. Phys. **47** (2008) 8003.